

What is claimed is:

1. A semiconductor structure comprising:
  - a semiconductor substrate having a strained layer-free region and a strained layer region;
  - a first device formed in the strained layer-free region of the semiconductor substrate; and
  - a second device formed in the strained layer region of the semiconductor substrate.
2. The semiconductor structure of claim 1, wherein the first device comprises a memory cell and the second device comprises an FET.
3. The semiconductor structure of claim 2, wherein the memory cell is a low-leakage DRAM cell and the FET is a MOSFET logic device.
4. The semiconductor structure of claim 1, wherein the strained layer region has a trench selectively formed in the substrate, and comprises: a SiGe layer formed in the trench, and an epitaxial silicon layer formed on the SiGe layer.
5. The semiconductor structure of claim 4, wherein the epitaxial silicon layer is from about 2.5 to about 10 nm thick.
6. The semiconductor structure of claim 4, wherein the SiGe layer is epitaxially grown.

7. The semiconductor structure of claim 4, wherein the strained layer region further comprises a spacer formed on a sidewall of the trench, the spacer isolating strain produced in the strained layer region from the strained layer-free region.
8. The semiconductor structure of claim 4, wherein the trench is from about 100nm to about 400nm deep.
9. A method for fabricating a semiconductor structure comprising the steps of:
  - a) providing a semiconductor substrate having a strained-layer free region;
  - b) forming a first device in the strained layer-free region of the semiconductor substrate;
  - c) selectively forming a strained layer region in the semiconductor substrate; and
  - d) forming a second device in the strained layer region.
10. The method of claim 9, wherein step (c) further comprises:
  - i) forming a trench having a bottom surface and a sidewall surface;
  - ii) forming a layer of SiGe in the trench; and
  - iii) forming a layer of silicon on the layer of SiGe.
11. The method of claim 10, wherein step (ii) comprises epitaxially growing the layer of SiGe.
12. The method of claim 10, wherein step (iii) comprises epitaxially growing the layer of silicon.

13. The method of claim 10, wherein the layer of silicon is from about 2.5 nm to about 10 nm thick.
14. The method of claim 10, wherein after step (i), forming a spacer on the sidewall surface.
15. The method of claim 9, wherein the first device comprises a memory cell and the second device comprises an FET.
16. The method of claim 15, wherein the memory cell is a low-leakage DRAM cell and the FET is a MOSFET logic device.